

What is claimed is:

1 1. A method comprising:

2 selectively coupling capacitors of oscillator stages together to set an oscillation frequency.

1 2. The method of claim 1, wherein the coupling comprises differentially coupling the

2 capacitors together.

1 3. The method of claim 1, wherein each stage comprises multiple capacitors, the

2 method further comprising:

3 selectively coupling the capacitors together in pairs to adjust the frequency.

1 4. The method of claim 3, further comprising:

2 binarily-weighting the capacitors.

1 5. The method of claim 1, wherein the coupling comprises:

2 coupling one terminal of a capacitor from each stage together and coupling the other

3 terminal of said capacitor from each stage to an output terminal.

1 6. The method of claim 1, further comprising:

2 selectively coupling the capacitors to ground.

1 7. The method of claim 6, wherein the selectively coupling the capacitors to ground

2 comprises:

3 coupling the capacitors to ground when not being used to adjust the oscillation frequency.

1 8. The method of claim 1, further comprising:
2 using one of the oscillator stages to generate a first output signal; and
3 using another one of a second signal orthogonal to the first signal.

1 9. The method of claim 8, wherein the first and second oscillating signals have the
2 oscillation frequency.

1 10. A system comprising:
2 a first oscillator stage;
3 a second oscillator stage; and
4 switches to selectively couple capacitors of the first and second oscillator stages together
5 to adjust an oscillation frequency.

1 11. The system of claim 10, wherein the switches differentially couple the capacitors
2 together.

1 12. The system of claim 10, wherein each stage comprises multiple capacitors,
2 wherein the switches selectively couple the capacitors together so that the capacitors when
3 coupled together are connected in a pair.

1 13. The system of claim 12, wherein the multiple capacitors are binarily-weighted.

1 14. The system of claim 10, wherein the switches couple one terminal of a capacitor
2 from each stage together and coupling the other terminal of said capacitor from each stage to an
3 output terminal.

1 15. The system of claim 10, further comprising:

2 additional switches to selectively couple the capacitors to ground.

1 16. The system of claim 15, wherein the switches selectively couple the capacitors to

2 ground that are not being used to adjust the oscillation frequency.

1 17. The system of claim 10, wherein:

2 the first oscillator stage generates a first output signal, and

3 the second oscillator stage generates a second signal orthogonal to the first signal.

1 18. A method comprising:

2 selectively activating capacitors to adjust an oscillating frequency of an oscillator; and

3 for each of the capacitors using parasitic capacitance as the main component of

4 capacitance for the capacitor.

1 19 The method of claim 18, further comprising:

2 forming the capacitors from parasitic capacitance exhibited between metal layers of a

3 semiconductor device.

1 20. The method of claim 18, further comprising:

2 forming the capacitors from metal-to-metal capacitors.

1 21. An apparatus comprising:

2 an oscillation stage; and

3 capacitors to regulate an oscillation frequency of an oscillator stage, the capacitors being

4 formed primarily from parasitic capacitance.

1 22. The apparatus of claim 21, further comprising:
2 forming the capacitors from parasitic capacitance exhibited between metal layers of a
3 semiconductor device.

1 23. The apparatus of claim 21, further comprising:
2 forming the capacitors from metal-to-metal capacitors.

1 24. A system comprising:
2 a oscillator stage;
3 a second oscillator stage;
4 switches to selectively couple capacitors of the first and second stages together to adjust
5 an oscillation frequency; and
6 a wireless interface to communicate with a communication link in response to at least one
7 oscillation signal provided by at least one of the first and second oscillator stages.

1 25. The system of claim 24, wherein the wireless interface comprises a dipole
2 antenna.